That which is claimed is:

1. A photomask for patterning an integrated circuit device using a patterning radiation, the photomask comprising:

a transparent substrate having first and second opposing surfaces;

a pattern of radiation blocking regions on at least one of the first and/or second surfaces of the transparent substrate, the pattern of radiation blocking regions defining a pattern to be transferred to the integrated circuit substrate; and

an array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate and wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the array of shadowing elements is greater than approximately 20%.

2. A photomask according to Claim 1 wherein a shadowing element of the array has an index of refraction that is different than that of an adjacent portion of the transparent substrate.

3. A photomask according to Claim 1 wherein an average of center-to-center spacings of the shadowing elements within the array is at least approximately 6μm.

4. A photomask according to Claim 3 wherein an average of center-to-center spacing of the shadowing elements within the array is at least approximately 8μm.

5. A photomask according to Claim 1 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the array of shadowing elements is greater than approximately 70%.

6. A photomask according to Claim 1 further comprising:

a second array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the second array has a light transmittance characteristic different than that of an adjacent portion

of the transparent substrate, wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the second array of shadowing elements is greater than approximately 20%, and wherein the transmittance of the patterning radiation through the portion of the transparent substrate including the second array is different than the transmittance of the patterning radiation though the portion of the transparent substrate including the first array.

7. A photomask according to Claim 6 wherein the first array of shadowing elements is configured to provide a first illumination condition for a first portion of the integrated circuit substrate and wherein the second array of shadowing elements is configured to provide a second illumination condition for a second portion of the integrated circuit substrate wherein the first and second illumination conditions are different.

8. A photomask according to Claim 7 wherein the first illumination condition comprises one of annular illumination, dipole illumination, or quadrapole illumination, and wherein the second illumination condition comprises another of annular illumination, dipole illumination, or quadrapole illumination.

9. A photomask according to Claim 6 wherein an average of center-to-center spacings of the shadowing elements within the first array is different than an average of center-to-center spacings of the shadowing elements within the second array.

10. A photomask according to Claim 9 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the first and second arrays of shadowing elements is greater than approximately 70%.

11. A photomask according to Claim 1 wherein the array of shadowing elements is configured to provide a holographic pattern used to generate a hologram on the integrated circuit device.

12. A photomask according to Claim 1 wherein the array of shadowing elements is configured as a fresnel lens.

13. A photomask according to Claim 1 wherein the pattern of radiation blocking regions comprises a pattern of a metal.

14. A photomask according to Claim 13 wherein the metal comprises chrome.

15. A photomask according to Claim 1 wherein a diameter of a shadowing element in the array is in the range of approximately 0.1μm to 4μm.

16. A photomask according to Claim 15 wherein a diameter of a shadowing element in the array is in the range of approximately 0.3μm to 1μm.

17. A method of forming a photomask for patterning an integrated circuit device using a patterning radiation, the method comprising;

providing a transparent substrate having first and second opposing surfaces;

forming a pattern of radiation blocking regions on at least one of the first and/or second surfaces of the transparent substrate, the pattern of radiation blocking regions defining a pattern to be transferred to the integrated circuit device; and

forming an array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate and wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the array of shadowing elements is greater than approximately 20%.

18. A method according to Claim 17 further comprising:

providing a pellicle on the transparent substrate prior to forming the array of shadowing elements wherein the array of shadowing elements is formed while maintaining the pellicle on the substrate.

19. A method according to Claim 17 wherein forming the array of shadowing elements comprises providing laser radiation to portions of the transparent substrate for a shadowing element of the array.

20. A method according to Claim 19 wherein forming the array of shadowing elements comprises providing a burst of laser radiation having a duration on the order of approximately 10^{-15} seconds for each of the shadowing elements of the array.

21. A method according to Claim 19 wherein forming the array of shadowing elements comprises providing a burst of laser radiation on the order of approximately 10^6 to 10^7 W/cm^2.

22. A method according to Claim 19 wherein providing laser radiation to portions of the transparent substrate for a shadowing element of the array generates a micro-explosion within the transparent substrate for the shadowing element of the array.

23. A method according to Claim 17 wherein a shadowing element of the array has an index of refraction that is different than that of an adjacent portion of the transparent substrate.

24. A method according to Claim 17 wherein an average of center-to-center spacings of the shadowing elements within the array is at least approximately 6μm.

25. A method according to Claim 24 wherein an average of center-to-center spacing of the shadowing elements within the array is at least approximately 8μm.

26. A method according to Claim 17 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the array of shadowing elements is greater than approximately 70%.

27. A method according to Claim 17 further comprising:

forming a second array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the second array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate, wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the second array of shadowing elements is greater than approximately 20%, and wherein the

transmittance of the patterning radiation through the portion of the transparent substrate including the second array is different than the transmittance of the patterning radiation though the portion of the transparent substrate including the first array.

28. A method according to Claim 27 wherein the first array of shadowing elements is configured to provide a first illumination condition for a first portion of the integrated circuit substrate and wherein the second array of shadowing elements is configured to provide a second illumination condition for a second portion of the integrated circuit substrate wherein the first and second illumination conditions are different.

29. A method according to Claim 28 wherein the first illumination condition comprises one of annular illumination, dipole illumination, or quadrapole illumination, and wherein the second type of illumination comprises another of annular illumination, dipole illumination, or quadrapole illumination.

30. A method according to Claim 27 wherein an average of center-to-center spacings of the shadowing elements within the first array is different than an average of center-to-center spacings of the shadowing elements within the second array.

31. A method according to Claim 30 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the first and second arrays of shadowing elements is greater than approximately 70%.

32. A method according to Claim 17 wherein the array of shadowing elements is configured to provide a holographic pattern used to generate a hologram on the integrated circuit device.

33. A method according to Claim 17 wherein the array of shadowing elements is configured as a fresnel lens.

34. A method according to Claim 17 wherein the pattern of radiation blocking regions comprises a pattern of a metal.

35. A method according to Claim 34 wherein the metal comprises chrome.

36. A method according to Claim 17 wherein a diameter of a shadowing element in the array is in the range of approximately 0.1μm to 4μm.

37. A method according to Claim 36 wherein a diameter of a shadowing element in the array is in the range of approximately 0.3μm to 4μm.

38. A method according to Claim 17 wherein forming an array of shadowing elements is performed prior to forming a pattern of radiation blocking regions.

39. A method of patterning an integrated circuit device, the method comprising:

providing an integrated circuit substrate having a photosensitive layer thereon;

projecting patterning radiation through a photomask to the photosensitive layer on the integrated circuit substrate, the photomask including,

a transparent substrate having first and second opposing surfaces,

a pattern of radiation blocking regions on at least one of the first and/or second surfaces of the transparent substrate, the pattern of radiation blocking regions defining a pattern to be transferred to the integrated circuit device; and

an array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate and wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the array of shadowing elements is greater than approximately 20%.

40. A method according to Claim 39 wherein a shadowing element of the array has an index of refraction that is different than that of an adjacent portion of the transparent substrate.

41. A method according to Claim 39 wherein an average of center-to-center spacings of the shadowing elements within the array is at least approximately 6μm.

42. A method according to Claim 41 wherein an average of center-to-center spacing of the shadowing elements within the array is at least approximately 8μm.

43. A method according to Claim 39 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the array of shadowing elements is greater than approximately 70%.

44. A method according to Claim 39 wherein the photomask further includes:

a second array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the second array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate, wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the second array of shadowing elements is greater than approximately 20%, and wherein the transmittance of the patterning radiation through the portion of the transparent substrate including the second array is different than the transmittance of the patterning radiation though the portion of the transparent substrate including the first array.

45. A method according to Claim 44 wherein the first array of shadowing elements is configured to provide a first illumination condition for a first portion of the integrated circuit substrate and wherein the second array of shadowing elements is configured to provide a second illumination condition for a second portion of the integrated circuit substrate wherein the first and second illumination conditions are different.

46. A method according to Claim 45 wherein the first illumination condition comprises one of annular illumination, dipole illumination, or quadrapole illumination, and wherein the second illumination condition comprises another of annular illumination, dipole illumination, or quadrapole illumination.

47. A method according to Claim 44 wherein an average of center-to-center spacings of the shadowing elements within the first array is different than an average of center-to-center spacings of the shadowing elements within the second array.

48. A method according to Claim 47 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the first and second arrays of shadowing elements is greater than approximately 70%.

49. A method according to Claim 39 wherein the array of shadowing elements is configured to provide a holographic pattern used to generate a hologram on the integrated circuit device.

50. A method according to Claim 39 wherein the array of shadowing elements is configured as a fresnel lens.

51. A method according to Claim 39 wherein the pattern of radiation blocking regions comprises a pattern of a metal.

52. A method according to Claim 51 wherein the metal comprises chrome.

53. A method according to Claim 39 wherein a diameter of a shadowing element in the array is in the range of approximately 0.1μm to 4μm.

54. A method according to Claim 53 wherein a diameter of a shadowing element in the array is in the range of approximately 0.3μm to 1μm.

55. A system for patterning an integrated circuit device using patterning radiation, the system comprising:

a chuck configured to receive an integrated circuit substrate having a photosensitive layer thereon;

a photomask including a transparent substrate having first and second opposing surfaces, a pattern of radiation blocking regions on at least one of the first and/or second surfaces of the transparent substrate the pattern of radiation blocking regions defining a pattern to be transferred to the integrated circuit substrate, and an array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the array has a light transmittance characteristic different than that of an adjacent portion of the

transparent substrate and wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the array of shadowing elements is greater than approximately 20%; and

a radiation source configured to project radiation through the photomask to the photoresist layer on the integrated circuit substrate.

56. A system according to Claim 55 wherein a shadowing element of the array has an index of refraction that is different than that of an adjacent portion of the transparent substrate.

57. A system according to Claim 55 wherein an average of center-to-center spacings of the shadowing elements within the array is at least approximately 6μm.

58. A system according to Claim 57 wherein an average of center-to-center spacing of the shadowing elements within the array is at least approximately 8μm.

59. A system according to Claim 55 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the array of shadowing elements is greater than approximately 70%.

60. A system according to Claim 55 further comprising:

a second array of shadowing elements within the transparent substrate between the first and second opposing surfaces wherein a shadowing element of the second array has a light transmittance characteristic different than that of an adjacent portion of the transparent substrate, wherein a transmittance of the patterning radiation through a portion of the transparent substrate including the second array of shadowing elements is greater than approximately 20%, and wherein the transmittance of the patterning radiation through the portion of the transparent substrate including the second array is different than the transmittance of the patterning radiation though the portion of the transparent substrate including the first array.

61. A system according to Claim 60 wherein the first array of shadowing elements is configured to provide a first illumination condition for a first portion of the integrated circuit substrate and wherein the second array of shadowing elements is

configured to provide a second illumination condition for a second portion of the integrated circuit substrate wherein the first and second illumination conditions are different.

62. A system according to Claim 61 wherein the first illumination condition comprises one of annular illumination, dipole illumination, or quadrapole illumination, and wherein the second illumination condition comprises another of annular illumination, dipole illumination, or quadrapole illumination.

63. A system according to Claim 60 wherein an average of center-to-center spacings of the shadowing elements within the first array is different than an average of center-to-center spacings of the shadowing elements within the second array.

64. A system according to Claim 63 wherein the transmittance of the patterning radiation through portions of the transparent substrate including the first and second arrays of shadowing elements is greater than approximately 70%.

65. A system according to Claim 55 wherein the array of shadowing elements is configured to provide a holographic pattern used to generate a hologram on the integrated circuit device.

66. A system according to Claim 55 wherein the array of shadowing elements is configured as a fresnel lens.

67. A system according to Claim 55 wherein the pattern of radiation blocking regions comprises a pattern of a metal.

68. A system according to Claim 67 wherein the metal comprises chrome.

69. A system according to Claim 55 wherein a diameter of a shadowing element in the array is in the range of approximately 0.1μm to 4μm.

70. A system according to Claim 69 wherein a diameter of a shadowing element in the array is in the range of approximately 0.3μm to 1μm.